REMARKS/ARGUMENTS

The office action of April 23, 2003 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-17 remain pending in this application. New claims 18-20 have been added.

Preliminarily, applicants note with appreciation the indication that the application contains allowable subject matter. Specifically, claims 11-15 have been allowed.

The Office Action states that the PTO Form 892, which formed part of paper 9 and identified U.S. Patent No. 5,708,382 to Park as being made of record, was attached to the Office Action. However, the document was not attached to the Office Action received by applicants. Thus, applicants kindly request the Examiner to again provide a copy of the PTO Form 892 making the Park patent of record with the next communication.

Claims 1, 2, 6, 7, 16 and 17 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent no. 5,319,253 to You. Claim 3 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over You. Claims 4, 5 and 8-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over You in view of U.S. patent no. 5,605,270 to D'Souza et al. ("D'Souza").

The action contends that You discloses all the features of independent claims 1, 6, 16 and 17. Referring to Fig. 6 of You, the action alleges that data retention enable mode circuit 100B and NOR gate 39 respectively show the clocked inverter circuit and logic circuit as recited in each of claims 1, 16 and 17. Also, the action asserts that the data retention enable mode circuit 100B and NOR gate 39 respectively show the inverter circuit and logic circuit called for in claim 6.

According to You, the output signal of the data retention enable mode circuit changes according to the input signal ϕWL when the data retention mode detection signal ϕDR supplied to the NAND circuit 35 in the data retention enable mode circuit 100B is at a high level. As a result, the circuit delays the voltage signal ϕN from the signal by time T3. When the data retention mode detection signal ϕDR supplied to the NAND circuit 35 in the data retention enable mode circuit 100B is at a low level the output signal from the data retention enable mode circuit 100B does not change irrespective of the input signal ϕWL. Thus, the data retention mode

detection signal ϕDR, and not the input signal ϕWL, controls when the output of the data retention enable mode circuit 100B changes. In contrast to You, the invention of amended claim 1 calls for a clocked inverter circuit to which a first pulse signal is supplied, *the clocked inverter circuit being controlled by the first pulse signal to output a second pulse signal* having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal. For at least this reason, claim 1 and dependent claims 2 and 3 are patentably distinct from You.

Amended claims 16 and 17 each call for the clocked inverter circuit being controlled by the first pulse signal to output a second pulse signal, and thus are considered patentably distinct from You for at least the same reasons as claim 1.

Claim 6 calls for, among other features, an inverter circuit *controlled by a clock signal* to which a first pulse signal is supplied, the inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width, the first pulse width being greater than a pulse width of the first pulse signal and the second pulse width being smaller than the pulse width of the first pulse signal. Contrary to the action's assertion, You does not teach or suggest an inverter circuit controlled by a clock signal. As discussed above with respect to You, the data retention mode detection signal ϕDR, and not the input signal ϕWL, controls when the output of the data retention enable mode circuit 100B changes. Since ϕDR is not a clock signal, claim 6 and dependent claim 7 are patentably distinct from You.

The action combines D'Souza with You to show the features of claims 4 and 5, which depend from claim 1, and claims 8-10, which depend from claim 6. Notwithstanding the propriety of the combination, D'Souza fails to remedy the deficiencies noted above with respect to You. Namely, D'Souza provides no teaching or suggestion of the clocked inverter circuit of claim 1 or the inverter circuit of claim 6. Thus, the combination of You and D'Souza, even if proper, does not result in the invention of claims 1, 4 and 5 or claims 6 and 8-10.

New claims 18-20 are fully supported by the specification and believed allowable over the art of record. For example, the art of record does not teach or suggest the first and second delay elements as called for in claims 18 and 19. Also, the art of record lacks a teaching or

suggestion of a clocked inverter circuit outputting a second pulse signal having one of a first pulse width and a second pulse width in response to a first pulse signal only.

CONCLUSION

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

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